The Eurasia Proceedings of Science, Technology, Engineering & Mathematics (EPSTEM)
ISSN: 2602-3199

The Eurasia Proceedings of Science, Technology, Engineering & Mathematics (EPSTEM), 2022

Volume 18, Pages 81-85

ICBASET 2022: International Conference on Basic Sciences, Engineering and Technology

Duty Cycle Detection Method for High Speed Input-Output Systems

Karen MELIKYAN
National Polytechnic University of Armenia (NPUA)

Abstract: A clock coupled duty cycle detection method for high speed input-output is presented in this paper. In High speed systems duty cycle (DC) of output signal needs to be calibrated at 50% for having acceptable performance in the system. The proposed method introduces a synchronous signal in the output of system with 50% duty cycle with maximum 1 % error over process, voltage, and temperature (PVT). Proposed method also compensate input referred offset of DC detector which helps to improve overall system performance. The duty cycle detection method was implemented in 16nm technology with a power supply of 1.2V. With this type of designed architecture, the circuit can provide up to 5Gbps frequency data signal. Experimental results show that proposed architecture is reliable, and it can work operative in high frequency intervals. The presented circuit can be implemented in special serial links of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB) and Double Data Rate (DDR).

Keywords: Duty Cycle, detector, high speed, calibration, process-voltage-temperature (PVT)

Introduction

The speed of many systems increases year by year. One of them are DDR systems (Wang, 2015) (Figure 1). Providing a good performance in them become more difficult. So, there arise problems with parameters, such us DC distortion, offset, jitter etc.

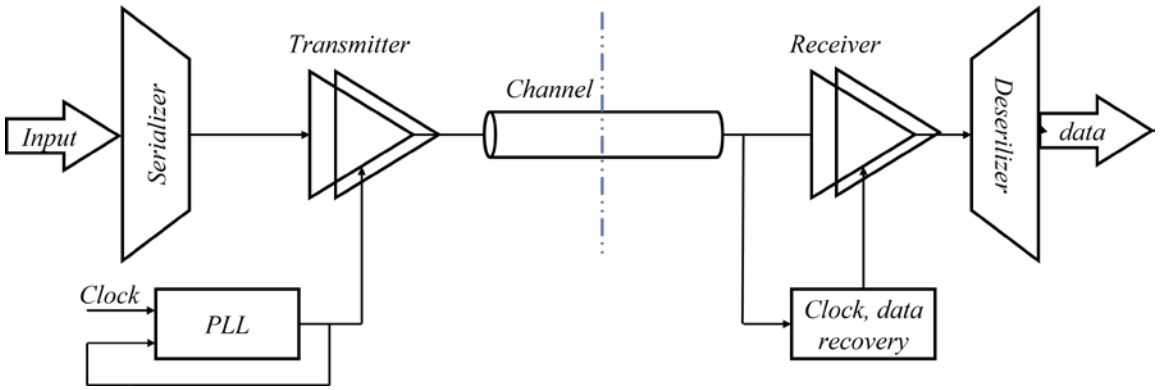

Figure 1. High speed system

Duty Cycle

DC is one of the most important parameters in high speed I/O circuit analyzes. If DC of circuit is not meet 50% specification, then we can have functional error, which can impact on data loss (Sindhu, 2015). DC signal basically measured (1) by pulse width (PW) and the period of signal components (Figure 2).

$$DC=(PW/Per) *100\% \quad (1)$$

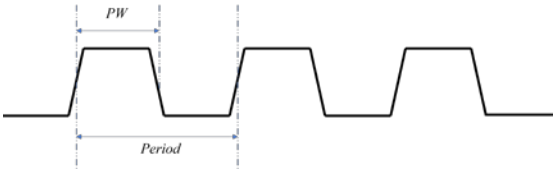

Figure 2. DC main components

Duty Cycle Detection Importance

The DC correction circuit (Melikyan, 2015) main blocks are adjuster and detector (Figure 3). The adjuster regulates a code for getting desired DC and send it to DC detector. The main function of detector is a correct measure of the DC error (%), make a right decision to send it to output and end operation, or continue corrective operation with sending signal to DC adjuster for requesting a new code.

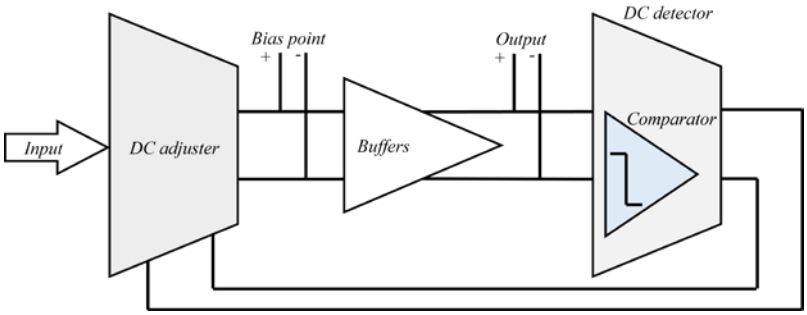

Figure 3. Block diagram of DC correction circuit

As nowadays circuits are working in the high frequency regions (Chien, 2019). The transistors and junctions in them get stressed while operating. So, for having acceptable performance in the system reliable architecture must be designed for DC detector, which can satisfy DC correcting circuit requirements.

Proposed Method of Duty Cycle Detection

Architecture of Duty Cycle Detector

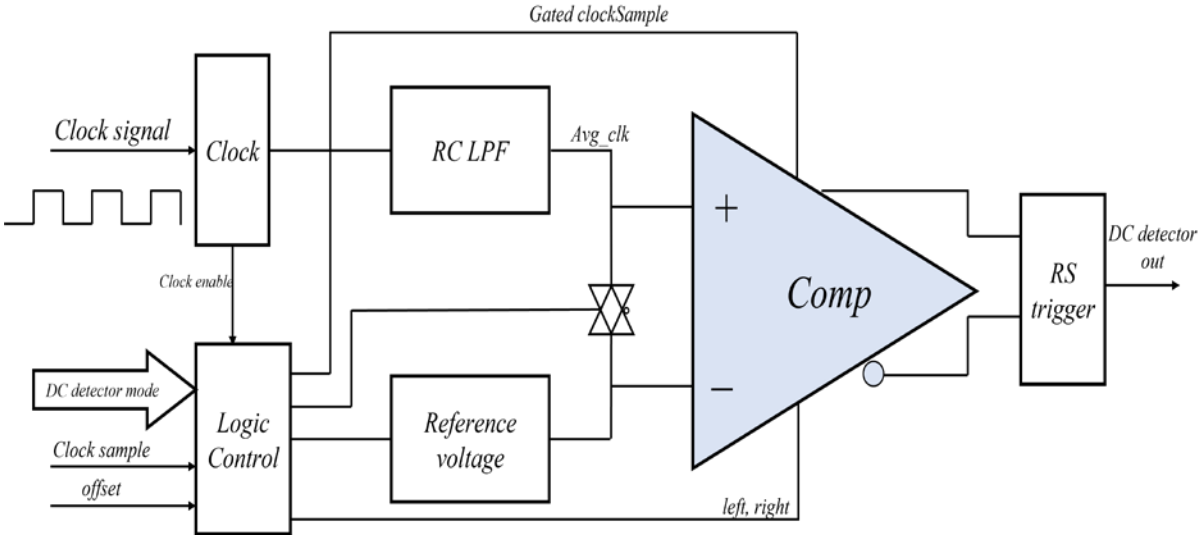

Figure 4. DC detector block diagram

The macro contains (Figure 4),

- digital control logic.
- analog DC detector core, including a mux for two input clocks, two RC tanks, and a comparator

The DC detector has two different functional modes: offset calibration mode and mission mode. The comparator offset is first calibrated in the offset calibration mode. Once it is done, the offset code is stored and used for the mission mode. In power down mode the analog DC detector is not measuring the incoming clock signals. The compactor is in the precharge mode with disabled offset legs. The two inverters are off and the two RC tank outputs are weakly driven to VSS.

Offset calibration mode: The offset code is incremented one by one to check when the comparator output toggles. The offset code is then stored and applied for the mission mode. It should be programmable between min and max code. The offset code either generated by the state-machine or can be overwritten by users. Also sweeping can't be wrapped around. It will be stopped at min or max value. Control and status register (CSR) default for the offset should be equivalent to no offset in the comparator.

The offset receive 5-bit binary code, MSB is the signed bit (1 is negative). Default and reset value is: 5'b00000 (this is the state of no offset). Min value is -15(5b'11111) and the max value +15(5b'01111). Mission mode: clk_sel chooses between the two input clocks. The average of the input clock signal is compared against the voltage divider output that is ideally at VDD/2. The comparator is either 1 or 0 depending on the relative relationship between the average clock and the reference voltage.

Operation Principle

The DC detecing algorithm is shown in block diagram (Figure 5). The Phase Locked Loop (PLL) provides the clock signal. Which pass trough RC filter, where clock signal become fixed in almost half of VDD level (~VDD/2). Logic cantrol block also is in level choosing mode, which will be fixed in the appropriate RC filter and value of signal becomes ~VDD/2. After both signals have been fixed in ~VDD/2 level they pass into key, which corrects offset code when ciruict works in offset mode.

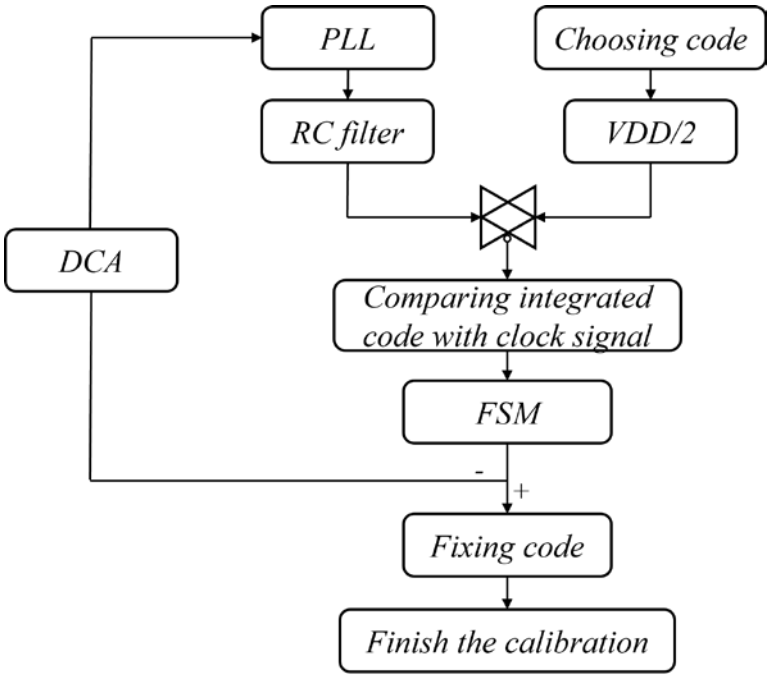

Figure 5. DC detector block diagram

In case of the mission mode the signal from PLL and choosed code get compared with each other to get information about signals level difference (error of DC detector), which must meet DC min/max error value specification. In the case when DC error is out of advisable specification of DC detector, finite state machine (FSM) enters the signal to DC adjuster block where the code will be changed and sent back to PLL block. FSM

passes the code and calibrates it until finding the best output signal. After getting acceptable performance FSM fixes code and finishes calibration.

Results and Discussion

Simulations have been performed using circuit level simulator Hspice for 20 PVT corners (Hspice, 2010), including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to evaluate DC detection and offset correction of system, for 5Gbps frequency.

After starting operation circuit enters phase of settling. In the moment when settling time was ended, clock signal and chosen code get the appropriate voltage levels, the DC detection phase starts. In the end of operation comparator detects the DC (%) with the error percentage. In Figure 6 are shown DC detection results for FF corner, which is the worst corner in this case (Cosmosscope, 2018).

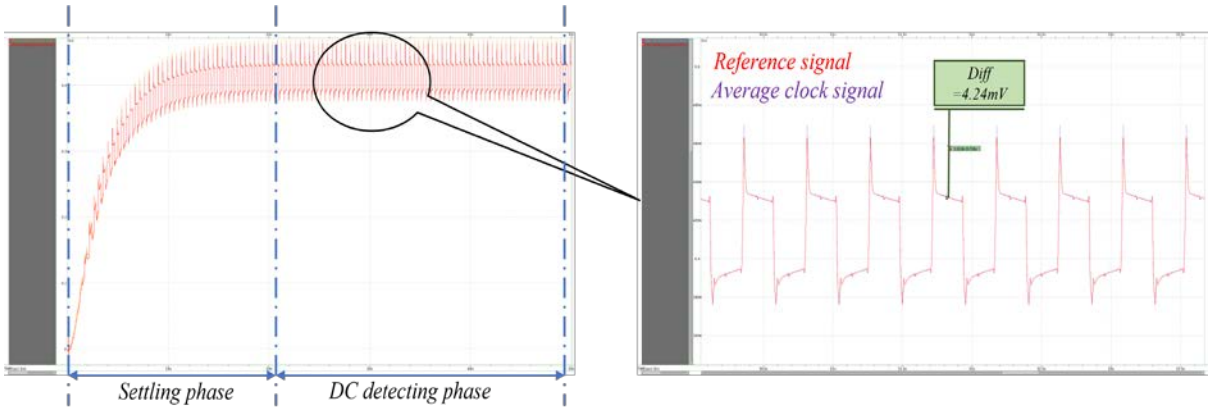

Figure 6. DC detected error in ff corner

In table 1 shown results of TT, FF and SS corners for DC and DC error min/max value.

Table 1. Simulation results for TT, FF, SS corners

Variables	Max difference on gate (mV)	DC detection max error (%)	DC (%)
TT	0.73	0.09	50.01
FF	4.24	0.54	50.61
SS	1	0.12	49.24

Conclusion

DC detection method designed for detecting error of DC in special high speed input-output systems. DC detection circuit used in method assist to maximum error and provide signals only with minimum DC error. The error maximum variation is 50%±1%. The architecture also corrects the offset of circuit with special offset mode implementing.

In high speed systems for 28nm and below processes it is hard to provide good performance without DC detection. So, this type of detection method is very important in special input-output circuits, due to huge PVT variations, which can have impact on the performance of the system. The approached method can be implemented for special input-output protocols of several standards such as DDR, USB, PCI.

Scientific Ethics Declaration

The author declares that the scientific ethical and legal responsibility of this article published in EPSTEM journal belongs to the author.

Acknowledgements or Notes

* This article was presented as an oral presentation at the International Conference on Basic Sciences, Engineering and Technology (www.icbaset.net) conference held in Istanbul/Turkey on August 25-28, 2022.

* This paper was supported by National Armenian Polytechnic University (NPUA). I thank my colleagues from Microelectronics and biomedical equipment departament, who provided insight and expertise that greatly assisted the research.

References

Chien, Y., L. & Heng, S., H. (2019). Design of a 0.8GHz-3GHz duty-cycle corrector with a 20%-80% input duty cycle. *IEEE International Conference on Consumer Electronics - Taiwan (ICCE-TW), 9*, 59-62.

Cosmosscope Reference Manual (2018), *Synopsys Inc*, 130.

Hspice Application Manual (2010), *Synopsys Inc.*,196.

Melikyan, V., Sahakyan, A., Hekimyan, A., Trdatyan, D., Shishmanyan, A. & Kazakhyan, T. (2015). Low power duty cycle adjustment simple method in high speed serial links. *IEEE East-West Design & Test Symposium (EWDTS)*, 1-4.

Sindhu, M. & Jamuna, V. (2015). Highly reconfigurable pulse width control circuit with programmable duty cycle. *2nd International Conference on Electronics and Communication Systems (ICECS)*, 2, 303-309.

Wang, X., & Hu, Q., (2015). Analysis and optimization of combined equalizer for high speed serial links. *IEEE 9th International Conference on Anti-counterfeiting, Security, and Identification (ASID), 9*, 43-46.

Author Information

Karen Melikyan
National Polytechnic University of Armenia
105 Teryan St, Yerevan, Armenia
Contact e-mail: *melikyan@synopsys.com*

To cite this article:

Melikyan, K. (2022). Duty cycle detection method for high speed input-output systems. *The Eurasia Proceedings of Science, Technology, Engineering & Mathematics (EPSTEM), 18*, 81-85.