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Design of a Reversible Full Adder Using Quantum Cellular Automata

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Abstract: Contemporary times holds a substantial hurdle in the designing of chips and ICs due to the roadblocks in the nanotech scaling of transistors, which is an obvious reason for Moore's Law to be working at a slower pace. The CMOS, VLSI technology imposes serious challenges when it enters the nano-domain, leading to the need of an innovation in nanotech scale. Quantum Dot Cellular Automata (QDCA or QCA) is a novel emerging transistor-less revolution for computation in the nanotech order. Besides this, irreversibility is a major concern in digital computation due to the loss of information. Therefore, here a reversible methodology is followed to address the problem of power dissipation. The purpose of this paper is to present a novel reversible full adder (RFA) of complexity 123 cells, 1.5 delay and area of 0.11 μm^2 is introduced using single layer cross over coplanar scheme, employing the demonstrated adder universal basic gates are implemented. On the basis of this adder we construct a 3-bit Comparator with a delay of 4.25 factors and cell count of 581.

Keywords: QCA, Reversible, gates, Reversible Full Adder(RFA), Power dissipation

Introduction

The notion of 'More Moore' talks about the persistent scaling of silicon-based CMOS transistors (Haron & Hamdioui, 2008). More and more a number of transistors can now be integrated on a single chip, but this has led to its own disadvantages, such as increase in leakage and tunneling current due to shrinking size (Haron & Hamdioui, 2008) and high-power dissipation. A reversible logic gate is one where there's no loss of energy. It has a uniform number of inputs and outputs. Following the bijective algorithm, it performs one to one mapping. The inputs or the outputs can easily be retrieved from one another and the main advantage is its almost zero power dissipation (Sen et al., 2014). The need to balance the number of inputs and outputs owing to Lindauer's principle (Sen et al., 2014) garbage outputs are utilized.

Reversible circuits are obtained from reversible gates. A reversible gate existing in nature is a NOT gate. Due to advancements in highly compact and dense nanoscale circuits, QCA technology is a viable alternative to Very Large-Scale Integration (VLSI) and Complementary Metal-Oxide Semiconductor (CMOS) technology. As a result, QCA technology operates at very low power and has a high switching speed in computational arithmetic and logical operations. (B.S et al., 2021). Hence due to the above-mentioned reasons, reversible gates are often designed using QCA technology for the best results. The ensuing sections of this paper illustrates the fundamentals of QCA, discussion about some existing full adders in literature, presenting a reversible full adder designed using QCA technology on QCA Designer (ver 2.0.3), simulation and implementation of universal gates with the proposed RFA and a comparator has been designed using this reversible full adder as a building block.

Fundamentals of QCA

Cell

Four quantum dots and two extra electrons, which can represent binary data, make up a standard QCA cell (Hashemi et al., 2018). The dots are placed opposite to one another and represent two stable states of polarization, -1 for logic “0” and +1 for logic “1”. Polarization of one cell depends on the polarization of the other (Figure 2.1a). QCA wire propagates the input to the output. (Figure 2.1b)

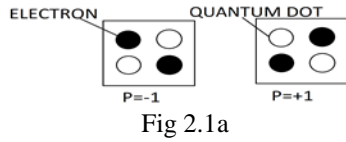


Fig 2.1a

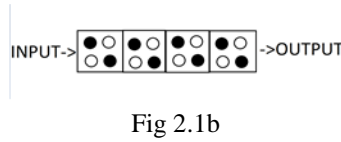


Fig 2.1b

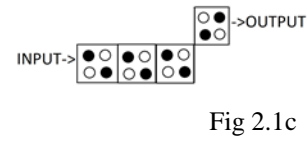


Fig 2.1c

Basic Gates in QCA

The operation of the five input majority gate (Figure 2.2a) is described by the formula: $OUT = MAJ5(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$ [4] and $Maj = MAJ3(a, b, c) = ab + bc + ac$, defines the functionality of 3-input majority gate (Abbasizadeh, & Mosleh, 2020) (Figure 2.2b). This gate behaves as an OR gate when the third output is changed to polarization state +1 and the same behaves as an AND gate if it is polarized to -1.

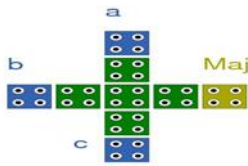


Figure 2.2a. MAJ3 gate

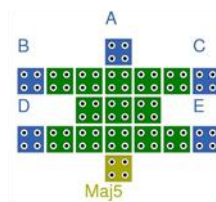


Figure 2.2b. MAJ5 gate

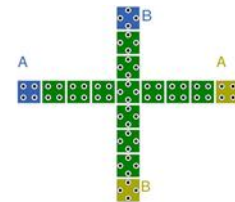


Figure 2.2c. Coplanar Crossover

Coplanar Crossover in QCA

Coplanar crossing occurs when two wires cross each other. The vertical cells need to be rotated by 45 degrees in order to propagate the correct information (Askari, & Taghizadeh, 2011). A is the input that goes to Y and B is the input that goes to X. In order for the input to be transmitted correctly, cells in the vertical plane should be rotated by 45 degrees.

Reversible Gates and Adders

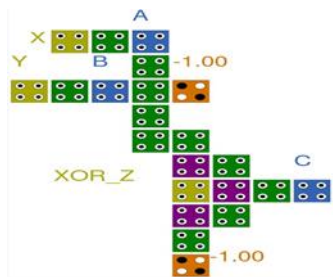


Figure 3. Toffoli gate

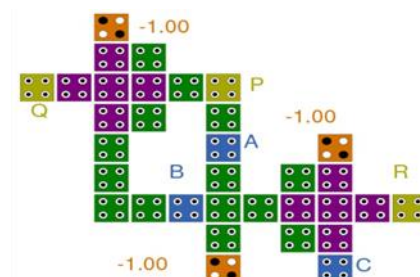


Figure 3b. Peres gate

The reason to work with reversible circuits is due to its minimum energy dissipation and relatively higher operating speed. Toffoli (Fig 3a), Peres (Fig 3b), Feynman, Double Feynman, Fredkin gate, CNOT are some of the standard reversible gates. The standard Toffoli and Peres gates are presented in (Patidar & Gupta, 2021; Bilal et al., 2017) respectively. In (Kianpour & Sabbaghi-Nadooshan, 2017; Taherkhani et al., 2017) designed reversible gate is used to implement an 8-bit adder-subtractor. (Taherkhani et al., 2017) has a lower garbage output and does not require the rotation of cells in comparison with (Kianpour & Sabbaghi-Nadooshan, 2017). In

Thapliyal et al., (2013) and Islam & Islam (2005), an efficient reversible carry looks ahead adder is demonstrated as a vital unit in effective computing. Babu et al., (2003), Islam & Islam (2003), Haghparast & Navi (2008), AnanthaLakshmi & Sudha (2013) are a few curated papers which investigate reversible gates. The table2 brings about the comparison between few existing reversible gates and the proposed RFA layout in terms of complexity, area and necessarily delay.

Proposed Full Adder

It so happens that preponderance of circuits performing addition and subtraction employs a full adder as a predominant integrant. Its aptness to combine the binary digits along with a carry in to churn out a carry out and sum has earned its reputation as such. The proposed reversible full adder (Figure 4) comprises 3 important gates, namely MAJ3, MAJ5 and a XOR gate. As shown in fig 4a the RFA includes 2 garbage outputs (G1, G2) and the other two outputs are carried and sum. Besides the 3 evident inputs A, B, C the fourth is a constant input D=0 during which the circuit behaves as a full adder, and at D=1 the sum remains same but however the carry is inverted opposite to what happens in case of D=0. The functionality of the demonstrated adder is as follows:

- $G1(\text{garbage}) = B$
- $G2(\text{garbage}) = C$
- $\text{CARRY} = \text{Maj}(A,B,C) \oplus D = D(\neg(\text{MAJ}(A,B,C))) + \neg D(\text{MAJ}(A,B,C))$
- $\text{SUM} = \text{Maj}(A,B,C, \neg(\text{MAJ}(A,B,C)), \neg(\text{MAJ}(A,B,C))) = \neg(\text{MAJ}(A,B,C))(A+B+C) + ABC$

Table 1. Truth table of Adder

D	A	B	C	G1	G2	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	1
0	0	1	1	1	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	1	1	1

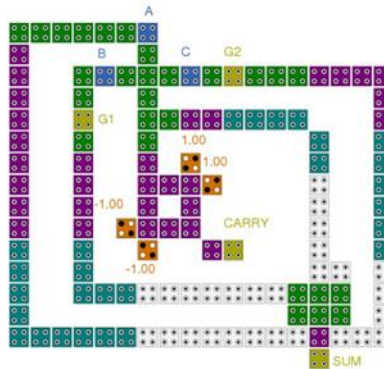


Figure 4. Proposed RFA

Implementation of the Proposed Full Adder as a Universal Gate

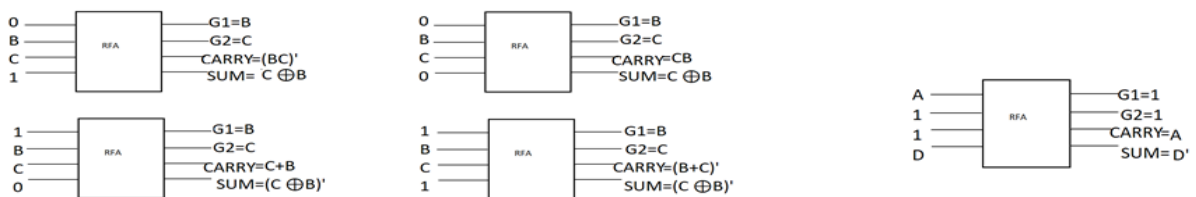


Figure 5a and Figure b. Implementation of the full adder as a universal gate

The proposed RFA is employed as different basic gates by changing the input combinations. The RFA performs all the universal operations: AND, NAND, OR, NOR, XOR, XNOR, Inverter. Figure 5a and Figure 5b shows the implementation of all the universal gates. Figure 5c shows the simulation of NAND and XOR gate.

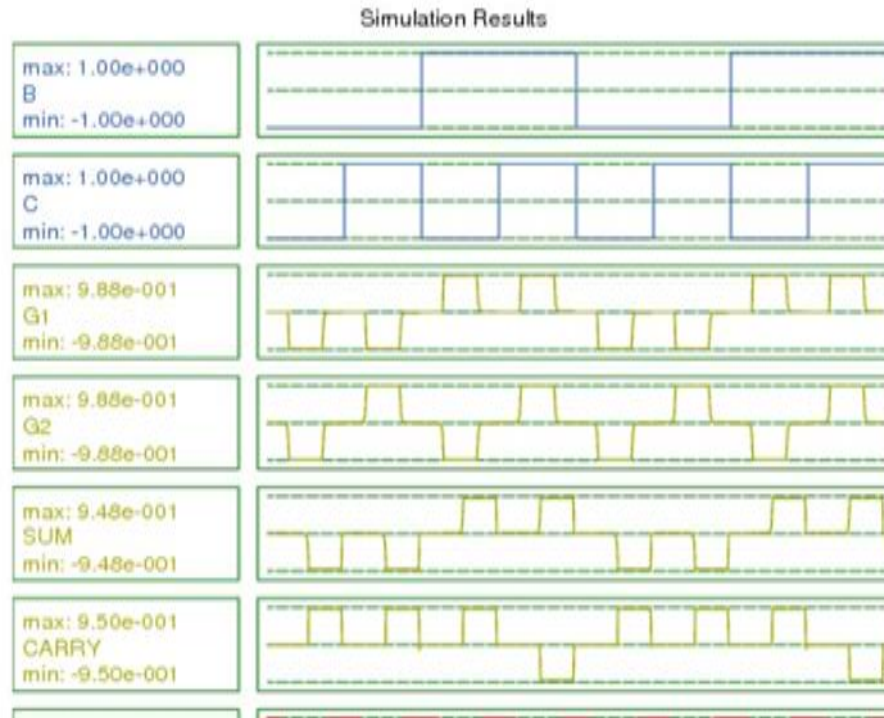


Figure 5c. Simulation for the combination 0 B C 1

Simulation and Comparison

Bi-stable approximation and coherence simulation engines are used to simulate and verify the proposed adder, signifying the adder's correctness. The RFA comprises 123 cells occupying an area of 0.11 μm^2 . The output SUM is delayed by a factor of 1.5, meanwhile the CARRY has a delay of about 0.5 following the negative edge of clock 1. The table (Table2) below demonstrates the performance of the few existing adders in the literature and the proposed one depending on the size, complexity (cell count), and latency. It is noticed that the proposed RFA is conducive with area, complexity, delay than the previous work (Hashemi et al ., 2018) although the functionality remains the same.

Table 2. Comparison of proposed RFA with existing

RFA	Area(μm^2)	Cells	Delay
Kianpour & Sabbaghi- Nadooshan (2017)	1.32	744	7.75
Taherkhani et al. (2017)	0.69	510	5
Thapliyal et al. (2013)	0.72	561	5
Babu et al. (2003)	0.47	305	3.2
Proposed RFA	0.11	123	1.5

Comparator

A comparator is an electronic circuit which compares the two applied inputs to generate a result indicating the relation between the inputs as greater, lesser or equal. A 3-bit comparator is designed using the proposed RFA. Comparators are used in applications in Analog to Digital converters and relaxation oscillations. The functionality of the comparator: $X > Y$ is detected as the carry out of the third adder, $X = Y$ is obtained by the AND operation of the sum obtained from 3 stages of the comparator, which is combined with $X > Y$ through a nor gate to generate $X < Y$. The complexity (cell count) of the implemented comparator is 581 with the area occupancy of 1.29 μm^2 , and the delay factor of the comparator is 4.25

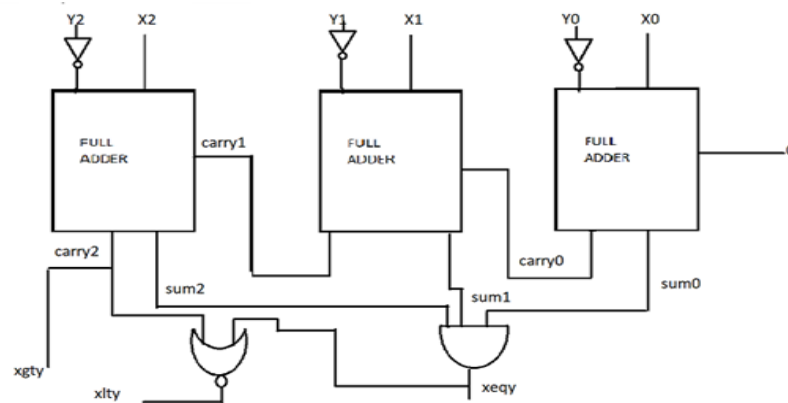


Fig.7a Comparator block diagram

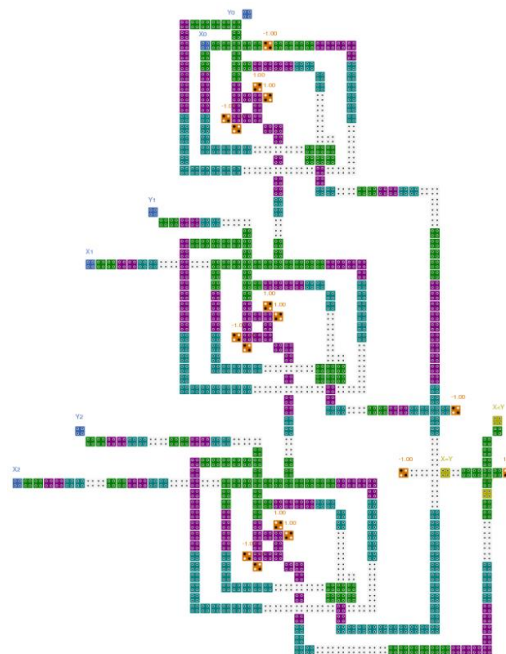


Fig.7b Comparator QCA implementation

Conclusion

This research work reports the design of a coplanar RFA for QCA applications. This design can easily be interfaced with other gates in larger designs. A comparator designed in this paper using the reversible full adder is found to have a delay at the cost complexity (cell count) 581. This can also be used as a universal gate as it is able to give results for every logical expression. The full adder design is more efficient than a lot of the existing designs as it occupies an area of $0.11\mu\text{m}^2$ and a delay of only 1.5. This design has created the path to simplify creation of many other circuits accurately and has led to the advancement of QCA technology.

Scientific Ethics Declaration

The authors declare that the scientific ethical and legal responsibility of this article published in EPSTEM journal belongs to authors.

Acknowledgements or Notes

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