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A New Nano-Design of an Efficient Synchronous Full-Adder/Subtractor Based on Quantum-Dots

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Abstract: Quantum-dot cellular automata (QCA), known as one of the alternative technologies of CMOS technology, promises to design digital circuits with extra low-power, extremely dense, and high-speed structures. Moreover, the next generation of digital systems will be used QCA as desired technology. In designing arithmetic circuits, efficient designs such as full-adder and full-subtractor can play a significant role. In addition, they are considering the most used structures in digital operations. Furthermore, full-adder and full-subtractor are always effective parts of all complex and well-known circuits such as Arithmetic Logic Unit (ALU), Microprocessors, etc. This paper proposes low complexity and high-speed QCA coplanar synchronous full-adder/subtractor structures by applying formulations based on the Exclusive-OR gate to decrease energy consumption. The proposed design is simulated using QCADesigner 2.0.3. The simulation results confirm the efficiency of the proposed circuit. Moreover, comparative investigation indicates the superiority of proposed designs compared to state-of-the-art designs. Finally, the suggested QCA coplanar synchronous full-adder/subtractor shows 5.88% and 7.69% improvement in consumed cells relative to the best full adder and full subtractor, respectively.

Keywords: Nanotechnology, Quantum-dot cellular automata (QCA), Coplanar; Full-adder; Full-subtractor, Nano-Electronic

Introduction

The enormous occupied area, short-channel effects, high power dissipation, slow speed, leakage current, etc., are still a few drawbacks of CMOS technology (Ahmadpour et al., 2020). Numerous investigations have been conducted at a Nano-scale to create digital circuits because this technology is constrained by physical limitations(Bahar et al., 2020). In order to overcome CMOS constraints, QCA is thought to be a promising revolutionary technique for the next generation of integrated circuits (ICs) (Angizi et al., 2014). Information in this technology is transmitted amongst electrons by Columbus contact since it has a lower density than CMOS (Bahar et al., 2020). Furthermore, since the lack of electrical currents, the circuits have rapid speeds, low occupied areas, and high densities (Bahar et al., 2019). Given these characteristics, numerous investigations on QCA-based circuits have been done (Liu et al., 2014). This method has been extensively applied to construct digital circuits like adders, multipliers, memory, multiplexers, etc. (Mustafa et al., 2013). The essential building block of mathematics, the QCA-cell, has four quantum dots at each of a square's four corners (Angizi et al., 2014). It also has two electrons that can be positioned at these dots and transferred via tunneling. Two crucial functions of clocking in QCA are to supply cells with energy and manage the circuit's data flow (Liu et al., 2014). Four crucial clocking phases form the foundation of QCA scheduling (Angizi et al., 2014).

The inverter gate (INV) and the majority voter (MV) are two commonly utilized foundation structures in this technology (Liu et al., 2014). The following are the characteristics of the current work:

- Proposing a new block diagram of QCA coplanar synchronous full-adder/subtractor for quantum-dots
- Proposing an efficient QCA coplanar synchronous full-adder/subtractor structure along with normal cells
- Evaluating the cell counts, complexity, and consumed area of the provided design to various cutting-edge designs.

The rest of the paper will discuss the following classification. Section 2 briefly introduces the QCA technology and related full adder/subtractor implementations. The proposed design of a new full adder/subtractor with the least amount of cells and complexity is the main topic of Section 3. Section 4 offers some last thoughts and a discussion of future directions.

Related Work

The adders in many computers and other kinds of processors are used. In addition, they are employed in other areas of the processor where they are utilized to compute table indexes, addresses, increment and decrement operators, and other related tasks. On the other hand, a full subtractor is a piece of electronic equipment or a logic circuit that can subtract two binary digits. In digital electronics, a combinational logic circuit is employed. In addition, Adders, encoders, decoders, and multiplexers are just a few of the integrated circuit devices that can be used to create combinational circuits. For the design of a full-adder by a 3-input XOR gate, Eqs. (1) and (2) can be used.

$$Carry_{out} = AB + BC + AC \quad (1)$$

$$Sum = A \oplus B \oplus C = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} \quad (2)$$

Table 1 presents a comparison of the previously proposed full adders concerning various criteria, including the number of majority gates, the quantity of inverting gate, delay, and the number of cells.

Table 1 the list of previously proposed full adders

Designs	#MV	#NOT	#Cell	Delay
Lent et al., 1994	5	3	192	NA
Wang et al., 2003	3	2	105	1
Sayedsalehi et al., 2015	3	2	105	0.75
Zhang et al., 2004	3	2	145	1
Kim et al., 2007	3	2	220	3
Hänninen et al., 2010	3	2	102	2

For the design of a full-subtractor by a 3-input XOR gate, Eqs. (3) and (4) can be used.

$$Bor = A\bar{B} + \bar{B}C + AC \quad (3)$$

$$Dif = A \oplus B \oplus C = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} \quad (4)$$

Table 2 presents a comparison of the previously proposed full-subtractor.

Table 2. List of previously proposed full-subtractors

Designs	#MV	#NOT	#Cell	Delay
Lakshmi et al., 2010	3	1	178	2
Dallaki et al., 2015	5	2	136	1.75
Reshi et al., 2016	2	1	104	1.75

Proposed synchronous full adder/subtractor

Synchronous full adder/subtractor is a prominent block in digital circuits. The most important disadvantages of circuits include high complexity, high latency and multi-layered structures. Hence, the recommended synchronous full adder/subtractor in QCA technology will be put into practice in this part. In addition, all simulations are performed using QCADesigner 2.0.3 simulator with default parameter values. We applied a

QCA-based XOR provided in (Ahmadpour et al., 2018) to construct an effective QCA architecture of the suggested QCA coplanar synchronous full-adder/subtractor. Based on interactions among cells, the XOR gate works. This gate's ability to simplify QCA structure design is one of its possible benefits. In the following, QCA coplanar synchronous full-adder/subtractor using 3-input exclusive-OR gate is designed. Suggested QCA coplanar synchronous full-adder/subtractor is merely composed of normal cells (not rotated). For the design of a synchronous full-adder/subtractor by a 3-input XOR gate, Eqs. (5),(6) and (7) can be used.

$$Cout = AB + BC + AC \tag{5}$$

$$Bor = A\bar{B} + \bar{B}C + AC \tag{6}$$

$$Dif = A \oplus B \oplus C = ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} \tag{7}$$

The truth table for the suggested QCA coplanar synchronous full-adder/subtractor is shown in Table 3.

Table 3. Truth table of suggested QCA coplanar synchronous full-adder/subtractor

A	B	C	Sum/Dif	Cout	Bor
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

Figure 1. Depicts the block diagram as well as the QCA layout of the suggested QCA coplanar synchronous full-adder/subtractor. It includes 96 total cells and occupies area of 0.1μm^2. Finally, it works in five clock cycles.

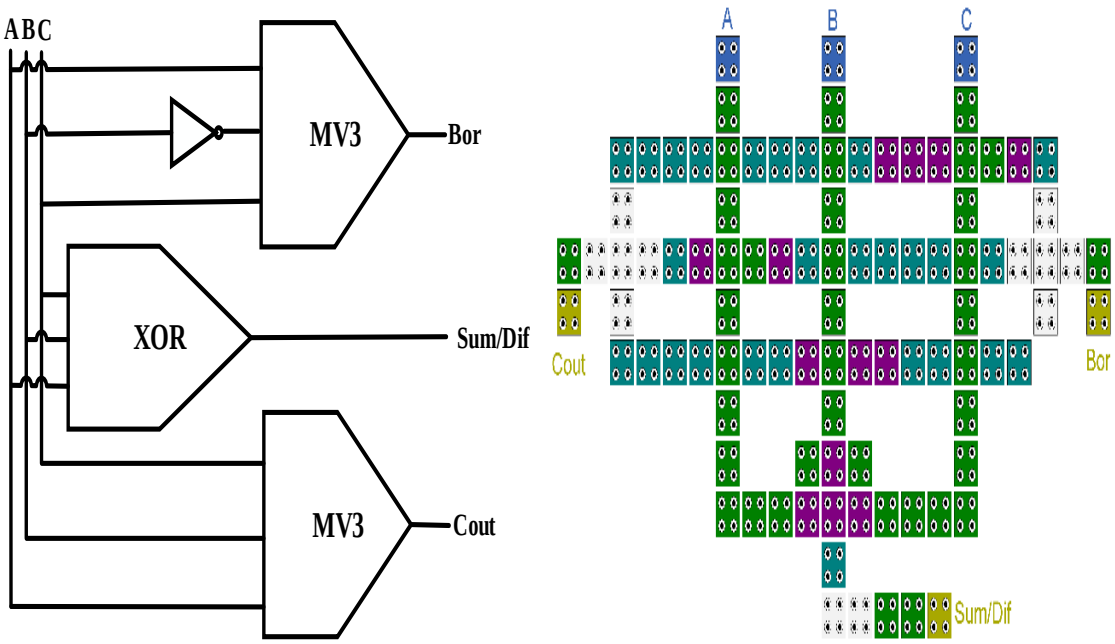

Figure 1**.** The proposed QCA coplanar synchronous full-adder/subtractor (a) circuit schematic (b) coplanar QCA layout

Resault and Discussion

In this section, we simulate the whole adder and subtractor designs for the proposed QCA with QCADesigner2.0.3. The QCADesigner software contains two simulation engines, called "Bistable Approximation" and "Coherence Vector," which should be mentioned [51]. In the QCADesigner software, every parameter and every simulation condition has default values. The simulation results of the proposed QCA-based full-adder for all combinations of inputs A, B, and C are shown in Fig. 2.

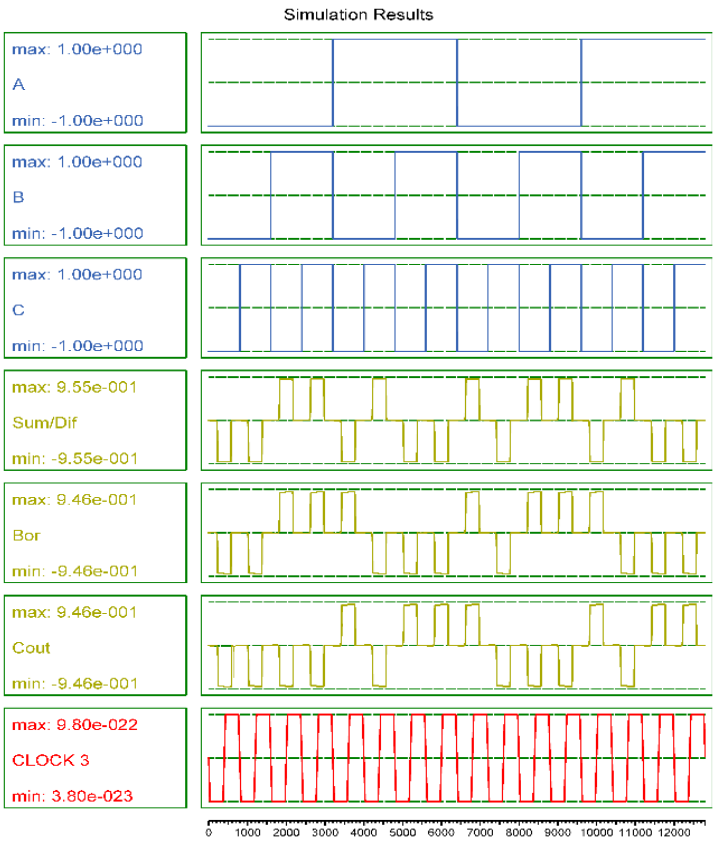

Fig. 2 Simulation results of the proposed coplanar QCA full-adder

Tables 4 and 5 compare all prior full-adder and full-subtractor designs with the proposed QCA coplanar synchronous full-adder/subtractor in terms of complexity (the number of required cells), number of majority gates, number of not gates, and clock latency (the number of required clock cycles).

Table 4. Evaluation for QCA- full adders.

Designs	#MV	#NOT	#Cell	Delay
Lent et al., 1994	5	3	192	NA
Wang et al., 2003	3	2	105	1
Sayedsalehi et al., 2015	3	2	105	0.75
Zhang et al., 2004	3	2	145	1
Kim et al., 2007	3	2	220	3
Hänninen et al., 2010	3	2	102	2
Proposed	3	2	96	1.25

Table 5. Evaluation for QCA full-subtractors.

Designs	#MV	#NOT	#Cell	Delay
Lakshmi et al., 2010	3	1	178	2
Dallaki et al., 2015	2	2	136	1.75
Reshi et al., 2016	2	1	104	1.75
Proposed	3	2	96	1.25

Power Dissipation Analysis

The Hartree-Fock approximation has been employed to estimate the power dissipation associated with only a QCA cell (Srivastava et al., 2011). The QCAPro tool was utilized to determine the energy dissipation of suggested QCA configurations (Srivastava et al., 2011). Table 6 lists the energy dissipation analysis outcomes for the recommended designs at three different tunneling energy levels (0.5 Ek, 1 Ek, and 1.5 Ek).

Table 6. Evaluation of the suggested design's energy consumption

In	Leakage Energy dissipated			Switching dissipated			Total energy dissipated		
	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K
Angizi et al., 2014	28	80	137	148	139	121	176	219	259
Abedi et al., 2015	16	49	89	103	89	78	120	138	168
Heikalabad et al., 2017	13	38	67	49	43	37	62	82	104
Balali et al., 2017	14	30	49	19	18	16	34	49	65
P	8	15	23	12	10	8	20	26	32

The suggested QCA coplanar synchronous full-adder/subtractor, as shown in Table 4, dissipates less power than the other specified designs.

Conclusion

The present study, proposed QCA coplanar synchronous full-adder/subtractor based on a 3-input QCA XOR gate. Moreover, the suggested QCA coplanar synchronous full-adder/subtractor showed 5.88% and 7.69% improvement in consumed cells relative to the best full adder and full subtractor, respectively. In addition, the evaluation of the power consumption was carried out using the QCAPro simulator. The analysis results of the suggested structure's power consumption compared with the best design at 0.5, 1, and 1.5 EK levels indicate a 41.17%, 46.93%, and 50.76% reduction in energy consumption, respectively.

Scientific Ethics Declaration

The authors declare that the scientific ethical and legal responsibility of this article published in EPSTEM journal belongs to the authors.

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