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SIMPLE REALIZATION OF MULTI-BIT RIPPLE CARRY ADDERS IN QCA TECHNOLOGY

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Abstract: An addition in digital signal processing is an important constructional unit for making all arithmetic operations. A full adder is a simple circuit that adds binary numbers. Ripple carry adder (RCA) is a cascade of the full adders that is used to add 8, 16, 32, etc. bit numbers. In this paper, multi-bit RCA is designed based on promising nanotechnology Quantum-dot Cellular Automata (QCA). In fact, QCA is getting investigated as an alternative to currently silicon-transistor based technology. The proposed RCA adder is designed as multilayer structure and is found as low complexity design in comparison with other RCA designs.

Keywords: Quantum-dot cellular automata, ripple carry adder, multilayer cross-over

Introduction

Current complementary metal oxide semiconductor (CMOS) technology has encountered serious challenges in terms of high-power consumption, feature size reduction and also leakage current problems. Quantum-dot Cellular Automata (QCA) is a promising nanotechnology that is considered as an alternative to CMOS technology. The main advantages of QCA are terahertz (THz) switching speed, low power consumption and ultra-small dimension features.

QCA is a transistor less technology, namely, is based on principle of quantum confinement. There are four dissimilar techniques for implementation of QCA, such as metal-island, semiconductor, molecular and magnetic QCA. Implementing QCA circuit is very difficult in room temperature, because to be found that operating only in cryogenic temperature. Recently, researchers (*G. A. DiLabio et al.*) have been able to successfully fabricate electrostatic QCA cell in room temperature. This invention is a great motivation for room temperature fabrication of QCA.

The fundamental unit of this technology is a QCA cell. It is square-shape tiny structure that consists of four quantum-dots and two excess electrons, as shown in Fig. 1(a). The electrons can travel among neighboring quantum dot space, but cannot leave the cell. The existing coulombic repulsion between the electrons forces them to be placed in opposite corner of the cell. Hence, there are only two stable states that represent the binary information “1” and “0”. A chain of QCA cells is a QCA wire. An inverter and majority gates play significant role as building blocks. Information propagation throughout the wires is controlled by QCA clocking. There are three types of wire-crossing techniques: coplanar crossover, multilayer crossover and logical crossover.

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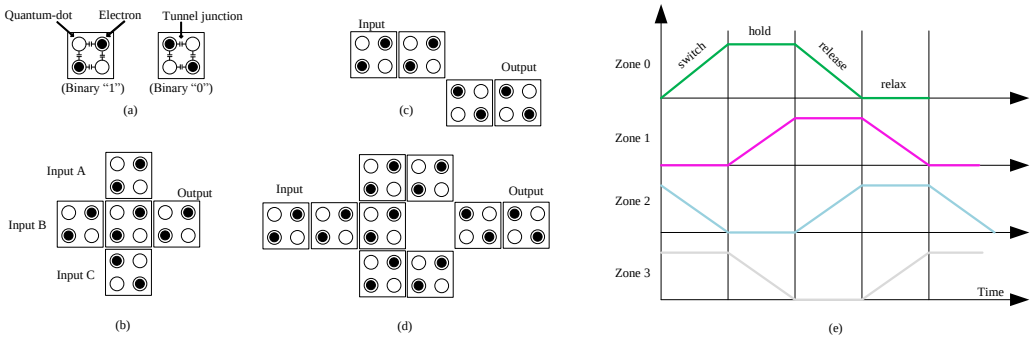

Figure 1. QCA Basics: (a) QCA Cell, (b) Majority Gate, (c) and (d) Inverter, (e) QCA Clocking

This paper focuses on RCA adder designs in QCA. In fact, RCA is constructed by cascading one bit full adder blocks serially. We use multilayer full adder to design RCA. Hence, the proposed RCA is also multilayer design and it gives us some achievements in terms of cell count, area and latency. We design 8-bit, 16-bit RCA designs with low complexity. Finally, we compare the proposed structures with previous works.

The Proposed Structures

In this section, we present multilayer QCA one-bit full adder (N. Safoev et al.) with its design process and by cascading serially the full adder, we design RCA adders. The proposed structures are designed as multilayer structures. The multilayer structures have some advantages in terms of area and delay aspects.

The one-bit full adder is a digital circuit that is used to add three binary numbers. Arithmetic operations: addition, subtraction, multiplication and division are implemented by using the full adder circuit. There are three input lines (A, B and C_{in}) and two output lines (Sum and C_{out}) in the circuit. An expression of the output is defined as follows:

$$\begin{aligned} Cout &= M(A,B,Cin); \\ Sum = XOR(A,B,Cin) &= M\big(M\big(A,\overline{B},Cin\big),M(A,B,\overline{Cin}\big),M(\overline{A},B,Cin)); \end{aligned} \quad (1)$$

In QCA technology, the majority gate of the three input lines expresses the output of "C_{out}" and an exclusive-OR (XOR) operation of the three input lines emphasizes the result of "Sum", as defined in Eq. (1). However, the majority gate based full adders were studied much in the previous works. The majority based full adder is implemented in accordance with Eq. (1), where "$M(\,)$" expresses majority gate. The problem is that each majority gate requires one clock phase in QCA.

After proposed five-input majority gates, QCA full adder based on that majority gate has been proposed. It has some advantages to design low complexity adder structures. A formulation of this full adder is expressed as follows:

$$Sum = 5 - M\big(\overline{Cout},\overline{Cout},Cin,A,B\big);$$

The one-bit full adder is implemented in QCA, as shown in Fig. 2(a) for designing n-bit QCA adders. The design of the presented full adder is a stereoscopic structure, because it has been designed in three layers, as indicated in Fig. 2(a). In the first layer, "C_{out}" is obtained using the majority gate. Summation (Sum) is obtained using QCA exclusive-OR gate in the third layer. Layer-two is a link layer between the layer-one and the layer-three.

A number of different structures for multi-bit adders have been proposed. The ripple carry adder (RCA) is found to be the simplest and smallest among them. A chain of n copies of the full adders represents the result of n-bit RCA circuit. Hence, we have designed RCA adder by connecting the full adders serially.

We propose 8-bit and 16-bit RCA designs based on QCA technology as shown in Fig. 3 and Fig. 4, respectively. Implementation of 8-bit RCA is achieved by sequential arrangement of eight 1-bit full adders. Inputs: $(A0,B0,C0),(A1,B1,C1)\ldots(A7,B7,C7)$ are feed to the adder blocks: Block-1, Block-2,… Block-8, respectively. Carry line of the previous block is feed to the next block for addition. Both of them are multilayer structures and note that there is no wire-crossing in the circuit. Multilayer technique is only used to obtain the result of summation.

The design of the proposed 8-bit RCA contains 436 cells with 0.35 μm^2 areas. The desired output is generated after 2.25 clock cycle. The next design 16-bit RCA structure occopys 1.2 μm^2 areas with a latency 4.25 clock cycle. There are not any inverters in the proposed structures. In that reason, complexity of the structures has been decreased. As a result, propagation delay aspect is also decreased simultaneously.

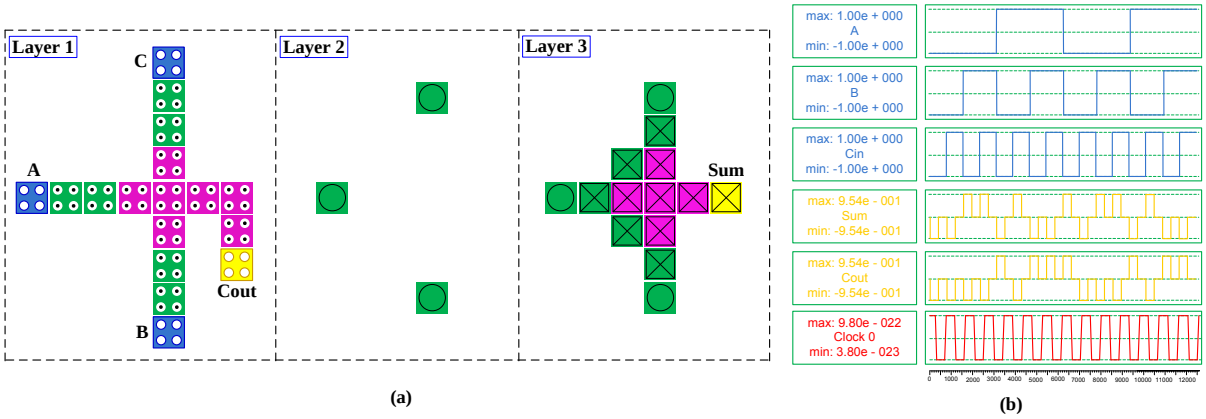

Figure 2. (a) Implementation of the full adder, (b) The simulation result

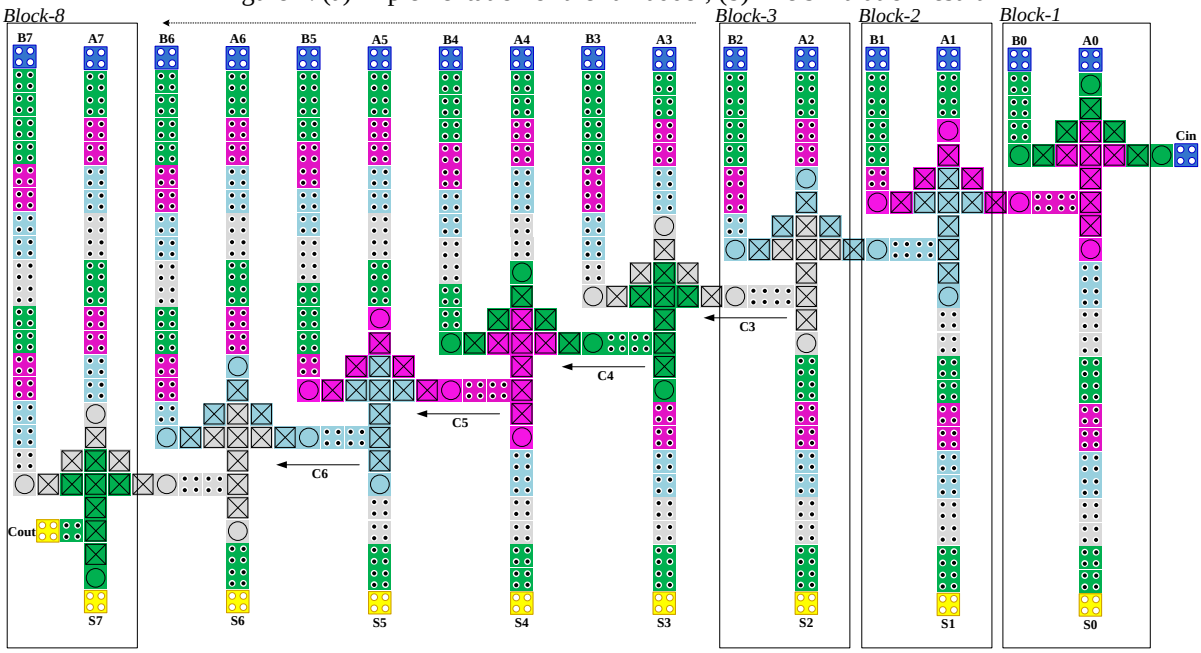

Figure 3. Implementation of the proposed 8-bit RCA

Results and Analysis

The functionality of the presented adders is carried out by QCADesigner tool version 2.0.3 (K. Walus et al.) which is accurate simulation tool for QCA circuit design. A bistable approximation engine is set to verify the functionality of the structure, parameters: 0.001 convergence tolerance, 65 nm radius effect, 12.9 relative permittivity, high clock 9.8e-022J, low clock 3.8e-023J, clock amplitude factor 2, layer separation 11.5 and maximum iterations per sample 100. The size of the cell is 18 nm. The simulation result of the full adder is given in Fig. 2(b). It confirms that the result of the full adder is correct and stable.

Table 1 shows a detail comparison between the proposed designs and previous ones in terms of cell count, area and latency aspects. According to the Table 1, the proposed structures have achieved significantly over the previous works. In the proposed RCA, carry line of the both designs is implemented by cascading the majority gates. Therefore, signal is propagated well due to a line of robust majority gates. Whole summation results of the RCA designs are obtained using the XOR gates directly.

In the comparison, the proposed 8-bit RCA has 24% improvement in terms of cell count over the previous best one (Abedi et al.) in the table. Fig. 5 indicates clearly illustration of comparison in the Table. 1.

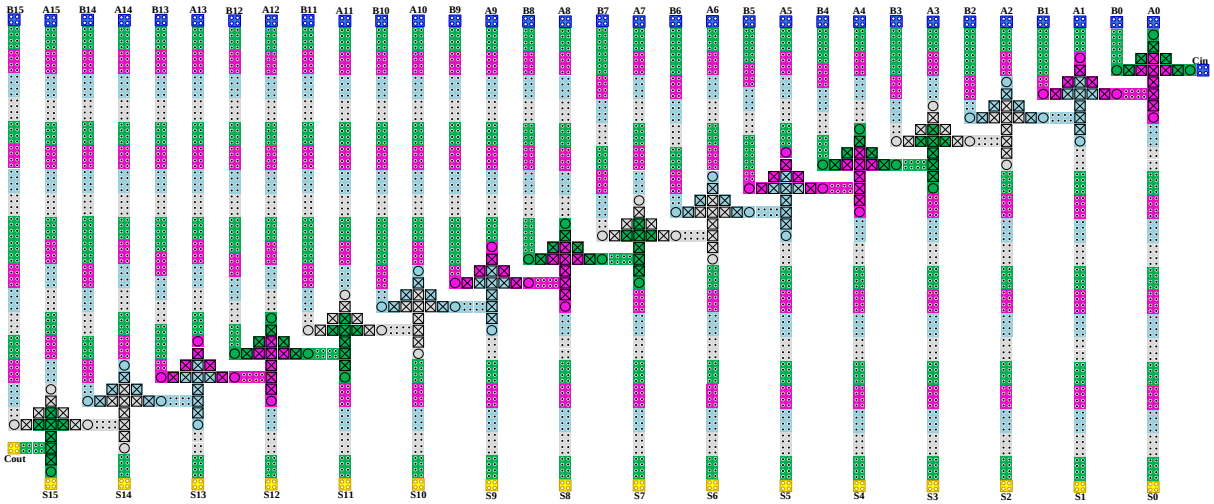

Figure 4. Implementation of the proposed 16-bit RCA

Table 1. Comparison table of the adders

	Circuits	Cell count	Area (μm^2)	Latency
8-bit RCA	Perri et al	1606	1.13	2.0
	Abedi et al	572	0.49	2.75
	Proposed	436	0.35	2.25
16-bit RCA	Perri et al	3587	2.66	3.0
	Abedi et al	1336	1.29	4.75
	Proposed	1284	1.2	4.25

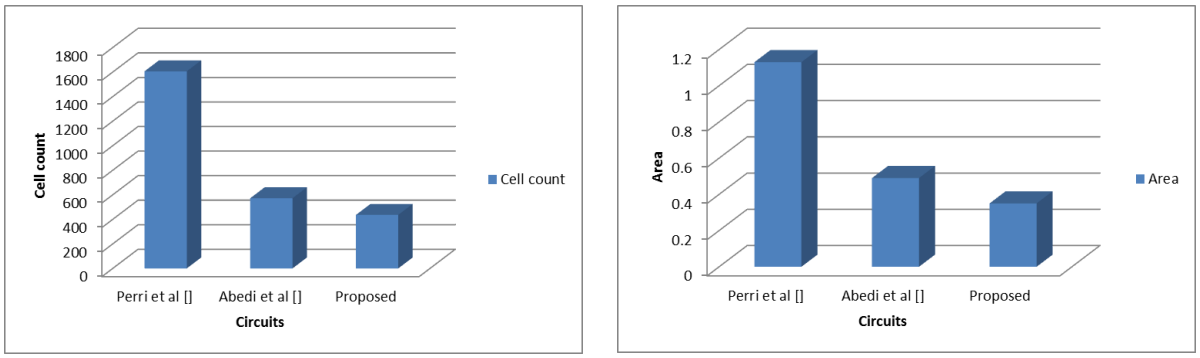

Figure 5. Comparison of QCA adder complexities

Conclusion

In this paper, we have proposed 8-bit and 16-bit RCA adders based on QCA. The functionality analysis has been carried out by QCADesigner tool and the results confirm that the proposed structures have correct and reliable output. The complexities of the proposed RCA designs have been compared with previous works and to be found that the proposed designs have significant improvements over prior works. The presented structures can be simply used in the design of QCA based arithmetic circuits.

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